

**Claims**

What is claimed is:

- 1 1. A substrate having an active side and a back side, comprising:
  - 2 an active side interconnect disposed on the active side;
  - 3 a backside interconnect disposed on the backside, coupled to and in substantial
  - 4 vertical alignment with the active side interconnect; and
  - 5 a redistributed interconnect of the backside interconnect disposed on the
  - 6 backside, coupled to and offset from the backside interconnect.
  
- 1 2. The substrate of claim 1, further comprising:
  - 2 a metal layer having a first side and a second side;
  - 3 a first dielectric layer adjacent to the first side of the metal layer;
  - 4 a first aperture in the first dielectric layer, the first aperture exposing a portion of
  - 5 the first side of the metal layer to define the active side interconnect;
  - 6 a second dielectric layer adjacent to the second side of the metal layer; and
  - 7 a via extending from the backside interconnect through the second dielectric
  - 8 layer to the second side of the metal layer to electrically couple the backside
  - 9 interconnect to the metal layer.
  
- 1 3. The substrate of Claim 1, wherein the redistributed interconnect comprises:
  - 2 a conductive trace coupled to and extending from the backside interconnect to a
  - 3 selected location;
  - 4 a third dielectric layer overlaying the conductive trace; and

5 an aperture in the third dielectric layer substantially at or near the selected  
6 location.

1 4. The substrate of Claim 3, wherein the selected location for the redistributed  
2 interconnect corresponds to an interconnect on a second substrate.

1 5. The substrate of Claim 1, wherein the redistributed interconnect is not in vertical  
2 alignment with the backside interconnect.

1 6. A semiconductor device, comprising:  
2 a carrier substrate having a bond pad;  
3 a first substrate, the first substrate comprising  
4 an active side and a back side;  
5 an active side interconnect, the active side interconnect disposed on the active  
6 side, coupled to the bond pad of the carrier substrate;  
7 a backside interconnect disposed on the back side, coupled to and in substantial  
8 vertical alignment with the active side interconnect;  
9 a redistributed interconnect of the backside interconnect, disposed on the  
10 backside, coupled to and offset from the backside interconnect; and  
11 a second substrate electrically coupled to the redistributed interconnect of the  
12 first substrate.

1 7. The semiconductor device of claim 6, wherein the first substrate comprises:

2 a metal layer having a first side and a second side;  
3 a first dielectric layer adjacent to the first side of the metal layer;  
4 a first aperture in the first dielectric layer, the first aperture exposing a portion of  
5 the first side of the metal layer to define the active side interconnect;  
6 a second dielectric layer adjacent to the second side of the metal layer; and  
7 a via extending from the backside interconnect through the second dielectric  
8 layer to the second side of the metal layer to electrically couple the backside  
9 interconnect to the metal layer.

1 8. The semiconductor device of Claim 6, wherein the redistributed interconnect  
2 comprises:

3 a conductive trace coupled to and extending from the backside interconnect to a  
4 selected location;  
5 a third dielectric layer overlaying the conductive trace; and  
6 an aperture in the third dielectric layer at the selected location.

1 9. The semiconductor device of Claim 8, wherein the selected location for the  
2 redistributed interconnect corresponds to an interconnect on the second substrate.

1 10. The semiconductor device of Claim 6, wherein the first substrate and the second  
2 substrates are microelectronic dies.

1 11. The semiconductor device of claim 6, wherein the second substrate is coupled to  
2 the redistributed interconnect by a process selected from the group including reflow  
3 bonding, thermal compression bonding or ultrasonic bonding.

1 12. The semiconductor device of Claim 6, wherein the redistributed interconnect is  
2 not in vertical alignment with the backside interconnect.

1 13. A method comprising:  
2 providing an active side interconnect to an active side of a substrate;  
3 providing a backside interconnect to a back side of the substrate with the  
4 backside interconnect being coupled to and in substantial vertical alignment with the  
5 active side interconnect; and  
6 providing a redistributed interconnect of the backside interconnect on the  
7 backside, the redistributed interconnect being coupled to and offset from the backside  
8 interconnect.

1 14. The method of Claim 13, wherein providing the redistributed interconnect  
2 comprises:  
3 depositing a conductive trace on the back side;  
4 coupling the conductive trace to the backside interconnect;  
5 extending the conductive trace to a selected location;  
6 placing a third dielectric layer over the conductive trace; and  
7 forming an aperture in the third dielectric layer at the selected location.

1 15. The method of Claim 13, wherein providing the backside interconnect comprises  
2 forming a via that extends from the backside interconnect through a second dielectric  
3 layer to a metal layer and filling the via with an electrically conductive material.

1 16. The method of claim 13, further comprising;  
2 providing a carrier substrate having a bond pad  
3 providing a second substrate having an interconnect;  
4 coupling the active side interconnect to the carrier substrate bond pad; and  
5 coupling the interconnect of the second substrate to the redistributed  
6 interconnect.

1 17. The method of Claim 16, wherein coupling the interconnect of the second  
2 substrate to the redistributed interconnect is performed by a process selected from the  
3 group including reflow bonding, thermal compression bonding or ultrasonic bonding.

1 18. A method for redistributing interconnects, comprising:  
2 providing a substrate having an active side and a backside, the active side  
3 having an active side interconnect;  
4 forming a via in the backside extending from a surface of the backside to a metal  
5 layer within the substrate;  
6 filling the via with an electrically conductive material such that a backside  
7 interconnect is formed at or substantially near the surface of the backside and in  
8 electrical communication with the metal layer;

9            depositing a conductive trace on the backside surface such that the conductive  
10 trace extends from the backside interconnect to a selected location on the back side  
11 surface;  
12            depositing a dielectric layer on the back side surface such that it overlays the  
13 conductive trace; and  
14            defining a redistributed interconnect of the backside interconnect at the selected  
15 location.

1    19.    The method of Claim 18, wherein defining the redistributed interconnect  
2 comprises forming an aperture in the dielectric layer at the selected location to expose a  
3 portion of the conductive trace.

1    20.    The method of Claim 19, wherein forming the aperture comprises etching a  
2 portion of the dielectric layer at the selected location to expose a portion of the  
3 conductive trace.

1    21.    The method of Claim 18, further comprising choosing the selected location to  
2 correspond to a location of a complementary interconnect of a substrate in facing  
3 relationship there with.

1    22.    The method of Claim 18, wherein depositing the conductive trace comprises  
2 forming a patterned electrically conductive layer on the backside surface using a  
3 photolithography process.

1 23. The method of Claim 18, further comprising depositing a conductive interconnect  
2 material into the dielectric aperture such that the conductive interconnect material is  
3 coupled to the redistributed interconnect and extends above the dielectric layer.

1 24. The method of claim 18, further comprising;  
2 providing a carrier substrate having a bond pad;  
3 providing a second substrate having an interconnect;  
4 coupling the active side interconnect to the carrier substrate bond pad; and  
5 coupling the interconnect of the second substrate to the redistributed  
6 interconnect.

1 25. The method of Claim 24, wherein coupling the interconnect of the second  
2 substrate to the redistributed interconnect is performed by a process selected from the  
3 group including reflow bonding, thermal compression bonding or ultrasonic bonding.